IN THE CLAIMS

Please amend the claims as follows:

1.-10. (Canceled).

11. (Previously Presented) A flip flop comprising:

a state retention portion to store a bit of digital data, said state retention portion having a first storage node and a second storage node; and

a clocking portion to transfer a new bit of digital data to said state retention portion in response to a clock signal, said clocking portion including:

a first stack of transistors coupled to said first storage node to draw current from said first storage node when a first digital data value is being transferred to said state retention portion, said first stack of transistors including a first transistor having a gate terminal coupled to receive said clock signal and a second transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal;

wherein said state retention portion includes a single latch and said single latch includes first and second inverters in a cross coupled configuration;

wherein said state retention portion includes a first pull up circuit connected between said first inverter and a power supply node and a second pull up circuit connected between said second inverter and said power supply node, said first pull up circuit having a first pull up transistor and a second pull up transistor connected in parallel to provide two separate pull up paths for said first inverter.

12. (Original) The flip flop of claim 11, wherein:

said first pull up transistor is larger than said second pull up transistor.

13. (Currently Amended) The flip flop of claim [3]11, further comprising:

a next state generation portion, connected to said clocking portion, to receive said new bit of digital data from an external source before it is transferred to said state retention portion by said clocking portion.

14. (Original) The flip flop of claim 13, wherein:

said next state generation portion includes at least one inversion device to invert a digital signal.

15. (Original) The flip flop of claim 14, wherein:

said next state generation portion includes an input node and a first inversion device connected between said input node and an end of said first stack of transistors.

16.-26. (Canceled)

27. (Previously Presented) A computing system comprising:

a digital processing device having at least one flip flop including:

a state retention portion to store a bit of digital data, said state retention portion having a first storage node and a second storage node, and

a clocking portion to transfer a new bit of digital data to said state retention portion in response to a clock signal, said clocking portion including a first stack of transistors coupled to said first storage node to draw current from said first storage node when a first digital data value is being transferred to said state retention portion, said first stack of transistors including a first transistor having a gate terminal coupled to receive said clock signal and a second transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal;

wherein said state retention portion includes a single latch and said single latch includes first and second inverters in a cross coupled configuration, wherein said state retention portion includes a first pull up circuit connected between said first inverter and a power supply node and a second pull up circuit connected between said second inverter

and said power supply node, said first pull up circuit having a first pull up transistor and a second pull up transistor connected in parallel to provide two separate pull up paths for said first inverter; and

a flash memory coupled to said digital processing device.

28. (Original) The computing system of claim 27, wherein:

said clocking portion further comprises a second stack of transistors coupled to said second storage node to draw current from said second storage node when a second digital data value is being transferred to said state retention portion, said second digital data value being different from said first digital data value, said second stack of transistors including a third transistor having a gate terminal coupled to receive said clock signal and a fourth transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal.

29. (Original) The computing system of claim 27, wherein:

said clocking portion comprises a clock node to receive said clock signal and an inversion device coupled between said clock node and said gate of said second transistor.

30. (Canceled)

31. (Previously Presented) The computing system of claim 27, wherein:

said first pull up transistor is larger than said second pull up transistor.

32. (New) The flip flop of claim 11, wherein said clocking portion further comprises:

a second stack of transistors coupled to said second storage node to draw current from said second storage node when a second digital data value is being transferred to said state retention portion, said second digital data value being different from said first digital data value, said second stack of transistors including a third transistor having a gate terminal coupled to receive said clock signal and a fourth transistor having a gate terminal coupled to receive a delayed, inverted version of said clock signal.

33. (New) The flip flop of claim 11, wherein:

said second pull up circuit includes a third pull up transistor and a fourth pull up transistor connected in parallel to provide two separate pull up paths for said second inverter.

34. (New) The flip flop of claim 33, wherein:

said third pull up transistor is larger than said fourth pull up transistor.

35. (New) The computing system of claim 27, wherein:

said second pull up circuit includes a third pull up transistor and a fourth pull up transistor connected in parallel to provide two separate pull up paths for said second inverter.

36. (New) The computing system of claim 35, wherein:

said third pull up transistor is larger than said fourth pull up transistor.